

What is claimed is:

1. A logical circuit designing device, comprising:
a logical circuit storage unit storing a logical
5 circuit;
a transmission line circuit generation unit
generating a transmission line circuit based on the
logical circuit stored in the logical circuit storage
unit; and
10 a transmission line circuit storage unit storing
the transmission line circuit generated by the
transmission line circuit generation unit.
2. A logical circuit designing device, comprising:
15 a logical circuit storage unit storing a logical
circuit;
a transmission line circuit storage unit storing
a transmission line circuit corresponding to the logical
circuit stored in the logical circuit storage unit;
20 a transmission line circuit editing unit editing
the transmission line circuit stored in the transmission
line circuit storage unit; and
a logical circuit modification unit modifying the
corresponding logical circuit based on the transmission
25 line circuit edited by the transmission line circuit

1.6.9.1
1.6.9.2
1.6.9.3
1.6.9.4
1.6.9.5
1.6.9.6
1.6.9.7
1.6.9.8
1.6.9.9
1.6.9.10
1.6.9.11
1.6.9.12
1.6.9.13
1.6.9.14
1.6.9.15
1.6.9.16
1.6.9.17
1.6.9.18
1.6.9.19
1.6.9.20
1.6.9.21
1.6.9.22
1.6.9.23
1.6.9.24
1.6.9.25
1.6.9.26
1.6.9.27
1.6.9.28
1.6.9.29
1.6.9.30
1.6.9.31
1.6.9.32
1.6.9.33
1.6.9.34
1.6.9.35
1.6.9.36
1.6.9.37
1.6.9.38
1.6.9.39
1.6.9.40
1.6.9.41
1.6.9.42
1.6.9.43
1.6.9.44
1.6.9.45
1.6.9.46
1.6.9.47
1.6.9.48
1.6.9.49
1.6.9.50
1.6.9.51
1.6.9.52
1.6.9.53
1.6.9.54
1.6.9.55
1.6.9.56
1.6.9.57
1.6.9.58
1.6.9.59
1.6.9.60
1.6.9.61
1.6.9.62
1.6.9.63
1.6.9.64
1.6.9.65
1.6.9.66
1.6.9.67
1.6.9.68
1.6.9.69
1.6.9.70
1.6.9.71
1.6.9.72
1.6.9.73
1.6.9.74
1.6.9.75
1.6.9.76
1.6.9.77
1.6.9.78
1.6.9.79
1.6.9.80
1.6.9.81
1.6.9.82
1.6.9.83
1.6.9.84
1.6.9.85
1.6.9.86
1.6.9.87
1.6.9.88
1.6.9.89
1.6.9.90
1.6.9.91
1.6.9.92
1.6.9.93
1.6.9.94
1.6.9.95
1.6.9.96
1.6.9.97
1.6.9.98
1.6.9.99
1.6.9.100

wherein

said transmission line circuit generation unit
generates a transmission line circuit based on the
topology information stored in the topology designation
5 table.

5. The logical circuit designing device according to
claim 1, further comprising

a value designation table storing a value of a
10 passive component composing a logical circuit, and
wherein

said transmission line circuit generation unit
generates a transmission line circuit based on the value
stored in the value designation table.

15

6. The logical circuit designing device according to
claim 1, further comprising

an addition designation table storing addition
information of a passive component composing a logical
20 circuit, and
wherein

said transmission line circuit generation unit
generates a transmission line circuit by adding the
passive component based on the passive component
25 addition information stored in the addition designation

7. The logical circuit designing device according to claim 1, further comprising

10 said transmission line circuit generation unit
generates a transmission line circuit by deleting the
passive component based on the passive component
deletion information stored in the deletion designation
table.

a topology designation table storing topology information indicating a type of a connection between active components composing a logical circuit, and

20 wherein

25

9. The logical circuit designing device according to claim 3, further comprising

a value designation table storing a value of a passive component composing a logical circuit, and

5 wherein

said transmission line circuit generation unit generates a transmission line circuit based on the value stored in the value designation table.

10 10. The logical circuit designing device according to claim 3, further comprising

an addition designation table storing addition information of a passive component composing a logical circuit, and

15 wherein

said transmission line circuit generation unit generates a transmission line circuit by adding the passive component based on the passive component addition information stored in the addition designation

20 table.

11. The logical circuit designing device according to claim 3, further comprising

a deletion designation table storing deletion information of a passive component composing a logical

25

2017/07/17

circuit, and

wherein

5 said transmission line circuit generation unit generates a transmission line circuit by deleting the passive component based on the passive component deletion information stored in the deletion designation table.

10 12. The logical circuit designing device according to claim 2, wherein

15 said logical circuit modification unit modifies the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

20 13. The logical circuit designing device according to claim 9, wherein

said logical circuit modification unit modifies the value of a passive component of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

25 14. The logical circuit designing device according to claim 10, wherein

Sub 3/1
Case 1
F01H01/00

PLANT	COL.	NO.	DATE	TIME	LOC.	REMARKS
1	1	1	1911	10:00	1000	1000
2	2	2	1911	10:00	1000	1000
3	3	3	1911	10:00	1000	1000
4	4	4	1911	10:00	1000	1000
5	5	5	1911	10:00	1000	1000
6	6	6	1911	10:00	1000	1000
7	7	7	1911	10:00	1000	1000
8	8	8	1911	10:00	1000	1000
9	9	9	1911	10:00	1000	1000
10	10	10	1911	10:00	1000	1000
11	11	11	1911	10:00	1000	1000
12	12	12	1911	10:00	1000	1000
13	13	13	1911	10:00	1000	1000
14	14	14	1911	10:00	1000	1000
15	15	15	1911	10:00	1000	1000
16	16	16	1911	10:00	1000	1000
17	17	17	1911	10:00	1000	1000
18	18	18	1911	10:00	1000	1000
19	19	19	1911	10:00	1000	1000
20	20	20	1911	10:00	1000	1000
21	21	21	1911	10:00	1000	1000
22	22	22	1911	10:00	1000	1000
23	23	23	1911	10:00	1000	1000
24	24	24	1911	10:00	1000	1000
25	25	25	1911	10:00	1000	1000
26	26	26	1911	10:00	1000	1000
27	27	27	1911	10:00	1000	1000
28	28	28	1911	10:00	1000	1000
29	29	29	1911	10:00	1000	1000
30	30	30	1911	10:00	1000	1000
31	31	31	1911	10:00	1000	1000
32	32	32	1911	10:00	1000	1000
33	33	33	1911	10:00	1000	1000
34	34	34	1911	10:00	1000	1000
35	35	35	1911	10:00	1000	1000
36	36	36	1911	10:00	1000	1000
37	37	37	1911	10:00	1000	1000
38	38	38	1911	10:00	1000	1000
39	39	39	1911	10:00	1000	1000
40	40	40	1911	10:00	1000	1000
41	41	41	1911	10:00	1000	1000
42	42	42	1911	10:00	1000	1000
43	43	43	1911	10:00	1000	1000
44	44	44	1911	10:00	1000	1000
45	45	45	1911	10:00	1000	1000
46	46	46	1911	10:00	1000	1000
47	47	47	1911	10:00	1000	1000
48	48	48	1911	10:00	1000	1000
49	49	49	1911	10:00	1000	1000
50	50	50	1911	10:00	1000	1000
51	51	51	1911	10:00	1000	1000
52	52	52	1911	10:00	1000	1000
53	53	53	1911	10:00	1000	1000
54	54	54	1911	10:00	1000	1000
55	55	55	1911	10:00	1000	1000
56	56	56	1911	10:00	1000	1000
57	57</					

✓

~~transmission~~

25 a logical circuit stored in a logical circuit database;

and

storing the generated transmission line circuit
in a transmission line circuit database.

5 18. A logical circuit designing method, comprising:
editing the transmission line circuit stored in
the transmission line circuit database; and
modifying a logical circuit corresponding to the
transmission line circuit based on the edited
10 transmission line circuit.

19. A logical circuit designing method, comprising:
generating a transmission line circuit based on
a logical circuit stored in a logical circuit database;
15 storing the generated transmission line circuit
in a transmission line circuit database
editing the transmission line circuit stored in
the transmission line circuit database; and
modifying the generated logical circuit based on
20 the edited transmission line circuit.

20. The logical circuit designing method according to
claim 17, wherein

the transmission line circuit is generated based
25 on topology information stored in a topology designation

SLA 4
Case 1:13-cv-00000-00000

table storing topology information indicating a type of a connection between active components composing a logical circuit, in said generating.

- 5 21. The logical circuit designing method according to claim 17, wherein

the transmission line circuit is generated based on a value of a passive component stored in a value designation table storing values of passive components
10 composing a logical circuit, in said generating.

22. The logical circuit designing method according to claim 17, wherein

the transmission line circuit is generated by
15 adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

20

23. The logical circuit designing method according to claim 17, wherein

the transmission line circuit is generated by deleting a passive component based on passive component
25 deletion information stored in a deletion designation

Table 4-29-60

Sub 191

sub A/

table storing deletion information of passive components composing a logical circuit, in said generating.

5 24. The logical circuit designing method according to claim 19, wherein

the transmission line circuit is generated based on topology information stored in a topology designation table storing topology information indicating a type
10 of a connection between active components composing a logical circuit, in said generating.

25. The logical circuit designing method according to claim 19, wherein

15 the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

20 26. The logical circuit designing method according to claim 19, wherein

the transmission line circuit is generated by adding a passive component based on addition information of the passive component stored in an addition
25 designation table storing addition information of

passive components composing a logical circuit, in said generating.

27. The logical circuit designing method according to
5 claim 19, wherein

Sub AG
the transmission line circuit is generated by deleting a passive component based on deletion information of the passive component stored in a deletion designation table storing deletion
10 information of passive components composing a logical circuit, in said generating.

28. The logical circuit designing method according to claim 18, wherein

15 the logical circuit is modified based on the transmission line circuit edited by said editing, in said modifying.

29. The logical circuit designing method according to
20 claim 25, wherein

the logical circuit is modified by modifying a value of a logical circuit stored in said logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

25

generating a transmission line circuit based on
a logical circuit stored in a logical circuit database;
and

34. A computer-readable storage medium which stores
a logical circuit designing program for enabling a
10 computer, comprising:

modifying a logical circuit corresponding to the
transmission line circuit based on the edited
15 transmission line circuit.

```

20         generating a transmission line circuit based on
        a logical circuit stored in a logical circuit database;

```

25 editing the transmission line circuit stored in
the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit.

5 36. The storage medium according to claim 33, wherein the transmission line circuit is generated based on topology information stored in a topology designation table that stores topology information indicating types of connections between active components composing a
10 logical circuit, in said generating.

37. The storage medium according to claim 33, wherein the transmission line circuit is generated based on a value stored in a value designation table storing
15 values of passive components composing a logical circuit, in said generating.

38. The storage medium according to claim 33, wherein the transmission line circuit is generated by
20 adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

25

FILED FOR

Sub A
cont

39. The storage medium according to claim 33, wherein
the transmission line circuit is generated by
deleting a passive component based on passive component
addition information stored in an addition designation
5 table storing deletion information of passive
components composing a logical circuit, in said
generating.

40. The storage medium according to claim 35, wherein
10 the transmission line circuit is generated based
on topology information stored in a topology designation
table storing types of connections between active
components composing a logical circuit, in said
generating.

41. The storage medium according to claim 35, wherein
the transmission line circuit is generated based
on a value stored in a value designation table storing
values of passive components composing a logical circuit,
15 in said generating.

42. The storage medium according to claim 35, wherein
the transmission line circuit is generated by
adding a passive component based on passive component
25 addition information stored in an addition designation

table storing addition information pf passive components composing a logical circuit, in said generating.

5 43. The storage medium according to claim 35, wherein
the transmission line circuit is generated by
deleting a passive component based on passive component
addition information stored in an addition designation
table storing deletion information of passive
10 components composing a logical circuit, in said
generating.

44. The storage medium according to claim 34, wherein
the logical circuit is modified based on the
15 transmission line circuit edited by said editing, in
said modifying.

45. The storage medium according to claim 41, wherein
the logical circuit is modified by modifying a
20 value of a logical circuit stored in said logical circuit
database based on the transmission line circuit edited
by said editing, in said modifying.

46. The storage medium according to claim 42, wherein
25 the logical circuit is modified by modifying

Sub A
Page 44 of 50

passive component addition information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

5

47. The storage medium according to claim 43, wherein the logical circuit is modified by modifying passive component deletion information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

48. The storage medium according to claim 44, wherein the logical circuit is modified based on a difference between a transmission line circuit by edited by said editing and a logical circuit stored in the logical circuit database, in said modifying.

49. A logical circuit designing program for enabling a computer, comprising:

generating a transmission line circuit based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit in a transmission line circuit database.

FIG. 4

5.17.1

50. A logical circuit designing program for enabling a computer, comprising:

editing the transmission line circuit stored in
5 the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit.

10 51. A logical circuit designing program for enabling a computer, comprising:

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit
15 in a transmission line circuit database;

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited
20 transmission line circuit.

52. The logical circuit designing program according to claim 49, wherein

the transmission line circuit is generated based
25 on topology information stored in a topology designation

Sub A.9
Case
F01260-103030

table that stores topology information indicating types of connections between active components composing a logical circuit, in said generating.

5 53. The logical circuit designing program according to claim 49, wherein

the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit,
10 in said generating.

54. The logical circuit designing program according to claim 49, wherein

the transmission line circuit is generated by
15 adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

20

55. The logical circuit designing program according to claim 49, wherein

the transmission line circuit is generated by deleting a passive component based on passive component
25 addition information stored in an addition designation

FIG. 10

Sub A11

table storing deletion information of passive components composing a logical circuit, in said generating.

5 56. The logical circuit designing program according to claim 51, wherein

the transmission line circuit is generated based on topology information stored in a topology designation table storing types of connections between active components composing a logical circuit, in said generating.

57. The logical circuit designing program according to claim 51, wherein

15 the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

20 58. The logical circuit designing program according to claim 51, wherein

the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive

Sal. A. 11
C. 11

FIG. 10

components composing a logical circuit, in said generating.

59. The logical circuit designing program according
5 to claim 51, wherein

the transmission line circuit is generated by deleting a passive component based on passive component addition information stored in an addition designation table storing deletion information of passive
10 components composing a logical circuit, in said generating.

60. The logical circuit designing program according to claim 50, wherein

15 the logical circuit is modified based on the transmission line circuit edited by said editing, in said modifying.

61. The logical circuit designing program according
20 to claim 57, wherein

the logical circuit is modified by modifying a value of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

25

62. The logical circuit designing program according to claim 58, wherein

the logical circuit is modified by modifying passive component addition information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

63. The logical circuit designing program according to claim 59, wherein

the logical circuit is modified by modifying passive component deletion information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

64. The logical circuit designing program according to claim 60, wherein

the logical circuit is modified based on a difference between a transmission line circuit by edited by said editing and a logical circuit stored in the logical circuit database, in said modifying.

65. A logical circuit designing device, comprising:
logical circuit storage means for storing a

See A131

[illegible]

5 means; and

transmission line circuit storage means for storing the transmission line circuit generated by the transmission line circuit generation means.